Novel IC layout parasitics analysis techniques to enhance Custom Macro/IP and Standard cell library development flow

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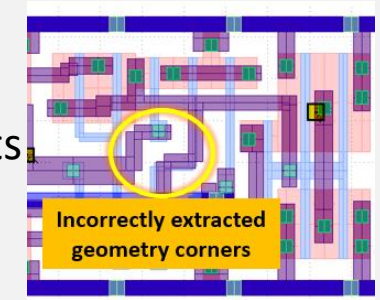
Motivation: Custom Macro/IP and Std. Cell library development flow challenges

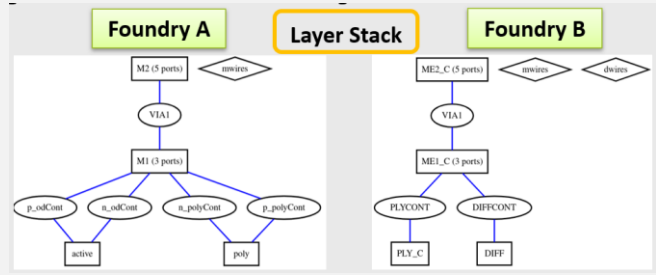
Visualization of macro/IP/standard cell Layout Parasitic Extraction (LPE) netlist to

- Get overview of design parasitics
  - especially, 3rd party vendor LPE netlists
- Ensure correct LPE netlist extraction by the extraction tool(s)



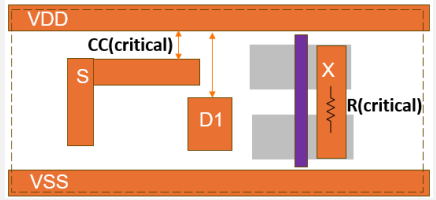
Compare two Foundries

- By comparing 2 LPE netlists - same design, different foundries



Identify Critical Resistance(R) and Coupling Capacitance(CC) in layout, with high probability of finding Latent defect

- Target Flow for fault analysis



Circuit Design → Layout → LPE → UDFM*

*UDFM: User defined Fault Model

Which parasitics impact the design behavior most?

- Accurately **locate** the design bottlenecks/parasitic elements (Net, Layer, co-ordinate)
- **Compare 2 LPE netlists**; locate and analyze the parasitics causing the difference

Parasitic Problems:

- P2P Resistance
- Ctotal
- CC
- RC delay
- Systematic layout mismatch

- Analyze design changes across layout revisions, PDK updates, LVS flow versions, extraction tools, and varying extraction options (e.g., temperature)

Limitation with previous approaches:

- manual, script-based: difficult to maintain/deploy
- used tools that were slow/difficult to setup/use
- did not sufficiently address our design challenges

1. Novel approach: Overview of layout parasitics

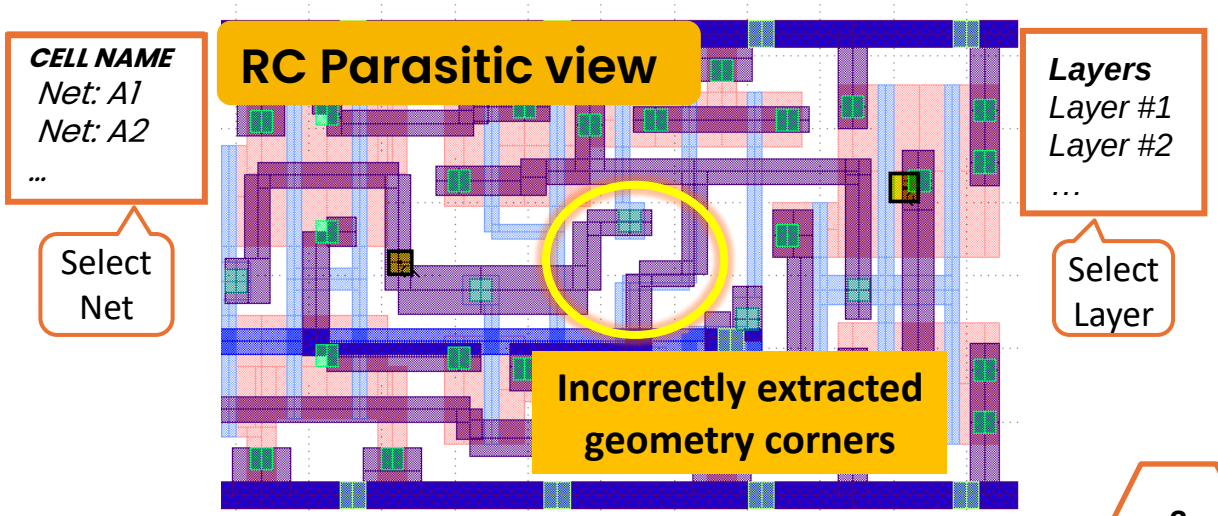
Visualization of the LPE netlist is the **new approach** that we have adopted to

- Understand layout connectivity; visualize design layers, RC parasitics and MOS devices
- Inspect 3rd party vendor **LPE** netlist, to check if
  - TAP cell is abutted to each Std. cell
  - GDS Overlay* were added to the IP/macro/std. cell design before LPE netlist is extracted

*GDS Overlay refers to extra layers/components added to account for change in characteristics (R, CC etc.) when IP/macro/std. cell design is instantiated in System-on-chip(SoC)

Result:

- 1 week effort saved per technology node compared to the previous approaches
- LPE netlist is no more a black-box !



Parasitics Visualization using the Ansys ParagonX

1. Novel approach: Overview of layout parasitics

Visualization of the LPE netlist is the new approach that we adopted to ensure

Extraction was done **properly** by standard extraction tools, esp. in 3rd party LPE netlists

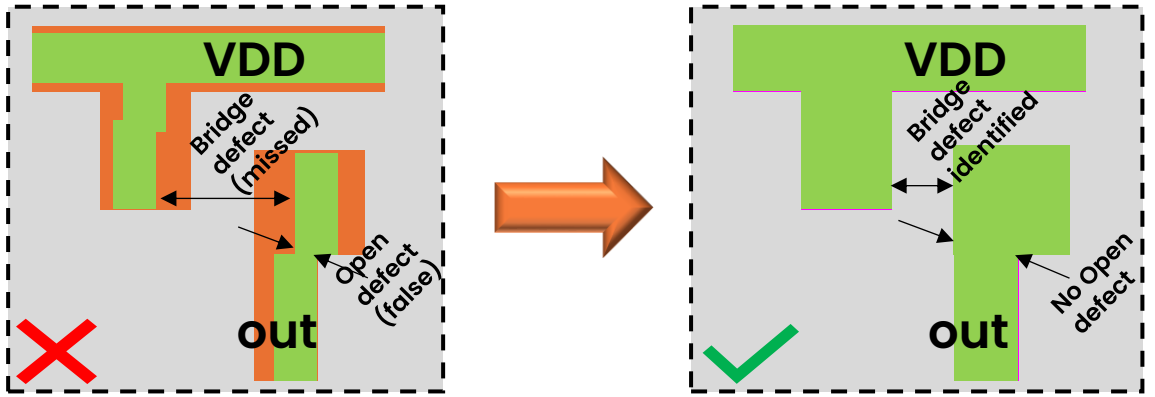
- power rails not missed
- critical nets (e.g. clocks) correctly extracted
- potential **Bridge defects not missed**
- **no false Open defects** reported due to incorrect extraction

Defects were located by overlaying original layout (GDS/AGF/OASIS) on visualized view of LPE netlist

- **Bridge/Short defect:** Unintended low resistance path between isolated nodes causes excessive current flow creating potential shorts during manufacturing
- **Open defect:** Space or opening in a conductor (like metals), preventing current flow

Result:

- Identify issues in 3rd party LPE netlists
- Avoid false and missed violations
- Identify and debug issues due to incorrect extraction of LPE netlist
- Saved **1 week** compared to previous approach

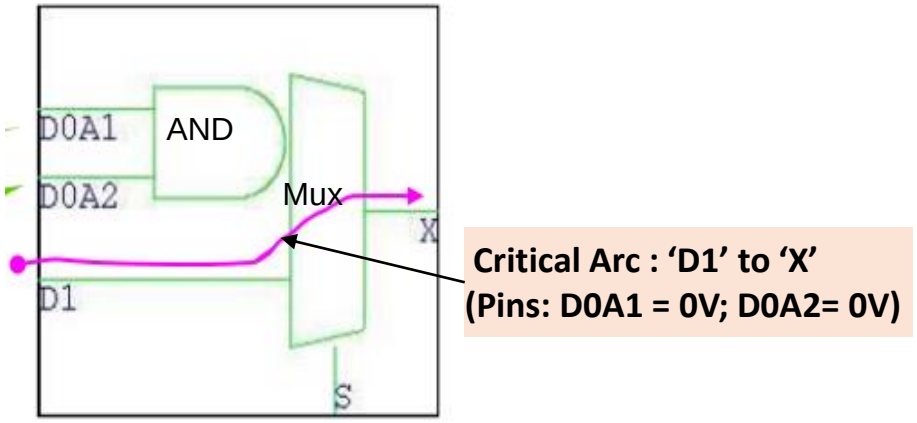


Incorrect LPE (Before)
(potential Bridge defect missed; reported False Open defect)

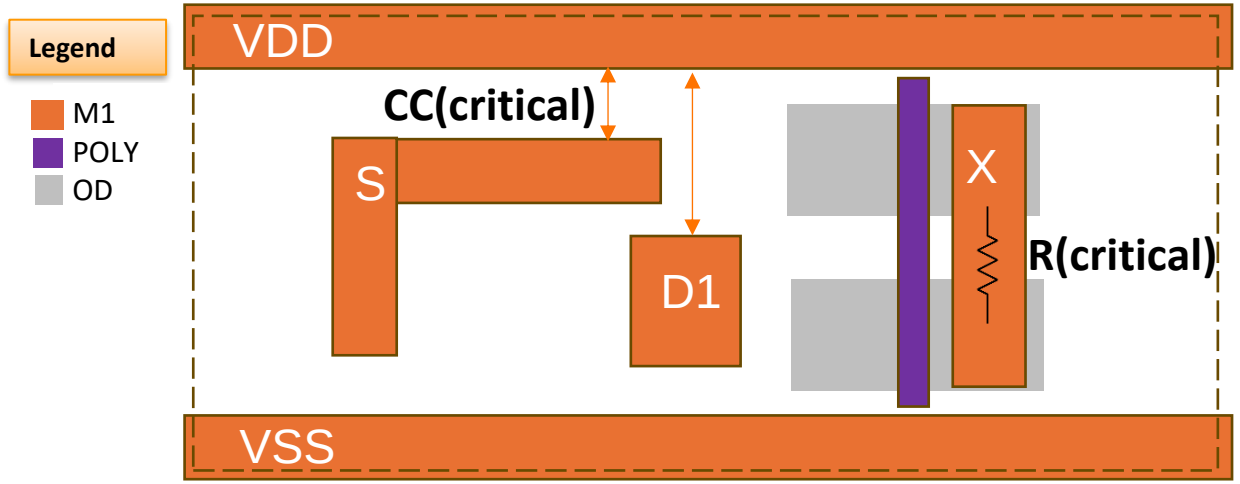
Correct LPE (After)
(Bridge defect detected; Open defect not reported)

2. Identify Critical R and CC to find Latent defect

- New and innovative approach for identifying Critical R and CC in the critical cell LPE netlist
  - First step towards locating latent defects
  - Such defects, defined using new UDFM vectors, added to existing Reliability test patterns/vectors



Critical cell: 2:1 MUX + AND in Register-to-Register (Reg2Reg) path



Critical R and CC identified using the Ansys ParagonX tool

Result: Critical R and CC values identified using ParagonX, modified in LPE netlist and simulated until Latent defects appear. New UDFM vectors, thus generated, added to existing DFT vectors to detect latent defects during **future reliability analyses.**

2. Identify Critical R and CC to find Latent defect

Reliability testing Flow

Select **critical timing paths** prone to failure.

E.g.: Reg2Reg data-path at target PVT condition

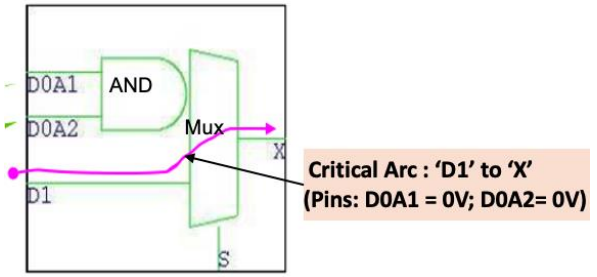
Select **critical cell** and **critical timing arc**, on critical timing path

Use ParagonX to identify critical R and CC in LPE netlist with high probability of finding Latent/cell internal defect

Perform “fault free” SPICE simulation with critical R and CC in LPE (**SIM_A**)

Perform “fault” SPICE simulation: Modify critical R and CC values in LPE and simulate until **Latent (Bridge/Open) defect** appears (**SIM_B**)

Compare **SIM_A** and **SIM_B** results to **generate extra UDFM patterns**



Critical cell: 2:1 MUX + AND in Register-to-Register (Reg2Reg) path

Bridge defect: a function of CC(critical)
Open defect: a function of R(critical)

Extra UDFM pattern,
*E.g.: [D0A1,D0A2,D1,S:X] = **[0000:0]***,
is added to the existing DFT vectors
E.g.: [D0A1,D0A2,D1,S:X] = {
*[1111:1], [1101:1], **[0000:0]**}*

3. Comparison: Foundry A vs Foundry B

AIM: To **select the right foundry** for our product

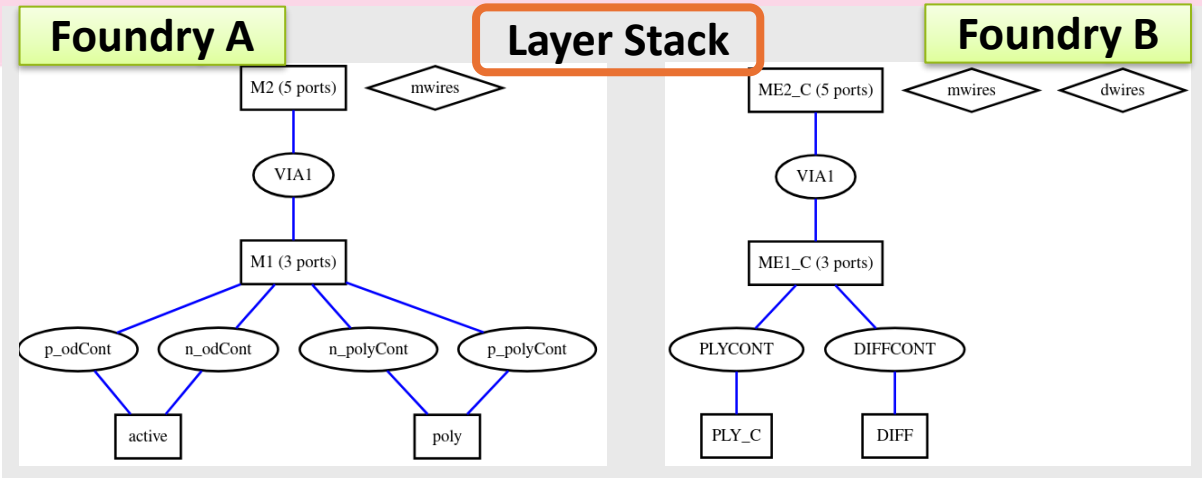
- Foundry B data compared against golden reference silicon proven data of Foundry A

Considerations: Timing signoff results (R and CC based), cost, …

- On LPE netlists (cell level xDSPF and design level SPEF), generated using Foundry A and B for the same design,
  - Compared average layer resistance(Av. R) and capacitance(Av. CC)
    - **Foundry B** found to have **much higher Av. CC** value

Result: **Selected Foundry A based on timing signoff results.**
Foundry B results did not match with Foundry A:

- Cell level (xDSPF): Huge differences in Av. R: 80% in Poly contact; 44% in VIA1
- Design level (SPEF): Significant difference in Av. CC: ~12% for 112,000 design nets



Cell level Resistance comparison

Layer	Foundry A – Av. R (Ohm)	Foundry B – Av. R (Ohm)	Av. R difference (Ohm)	Av. R difference (%)
Via 1	8	4.5	3.5	44
Poly contact	533	104	431	80

Design level Capacitance comparison

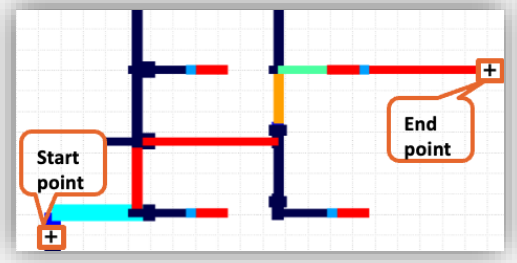
Foundry A – Av. CC (F)	Foundry B - Av. CC (F)	Av. CC difference (F)	Av. CC difference (%)
3.73E-15	4.18E-15	4.44E-16	12 %

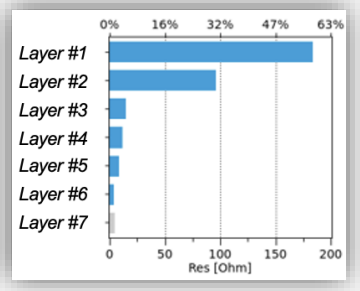
All above Results were generated using Ansys ParagonX tool

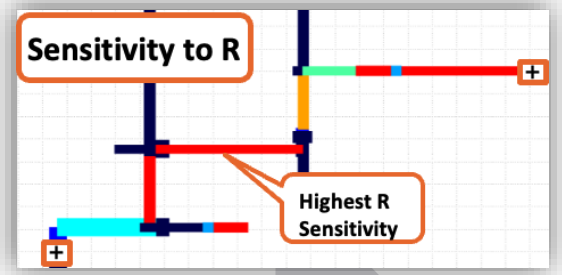
4. Locate Parasitic Bottlenecks impacting Design

We performed **Resistance (R) simulations to**

1. Precisely locate design geometries contributing highest resistance
   - by net, layer and co-ordinate







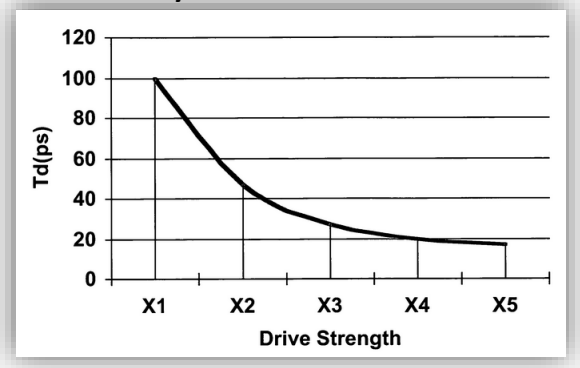
R Simulation on a net

Layer-wise contribution to total R

Sensitivity Analysis for R optimization

ParagonX uses **Heat map** to show the most sensitive polygons:
Red ➔ Highest sensitivity; **Blue** ➔ Least sensitivity

2. Compare custom Macro/IP current profile
   - same cell family, different drive strengths



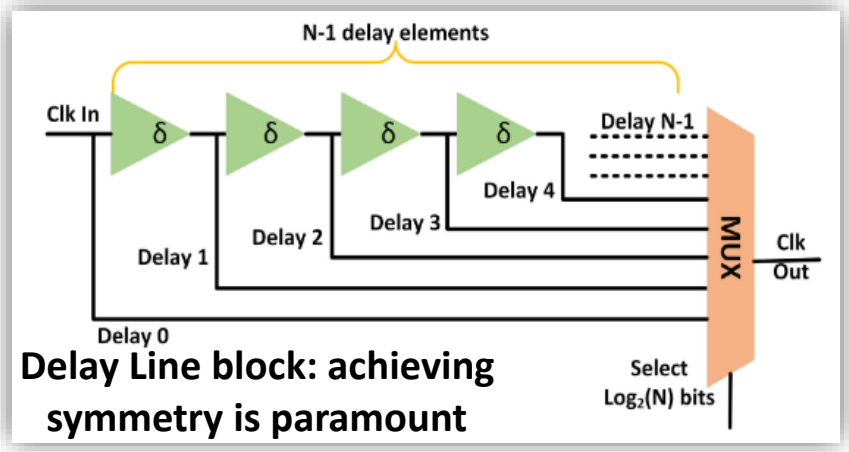
3. Perform PDK impact analysis
   - Check if PDK coded properly
   - Identify layers with highest R contribution
   - Verify min/max R in PDK using ParagonX

Result: Resistance simulation and sensitivity analysis using Ansys ParagonX helped us
1. accurately identify bottlenecks in via/metal layers in critical design nets
2. ensure that the custom macro current profiles were within specification
3. validate our updated PDK for correctness of R values, potentially saving 6 months of rework

4. Locate Parasitic Bottlenecks impacting Design

AIM: Identify **critical parasitic elements (net/layer/polygon)** of custom macro/IP, with high RC delay.

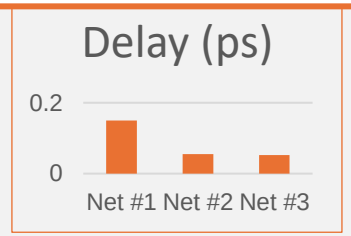
- Understand the root **cause of RC Delay**
  - Is RC delay due to net CC or net R or both?



Delay Line block: achieving symmetry is paramount

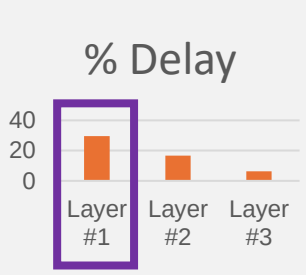
Net CC Contribution to total RC delay

Aggressor	Delay (ps)
Net #1	0.15
Net #2	0.055
Net #3	0.052



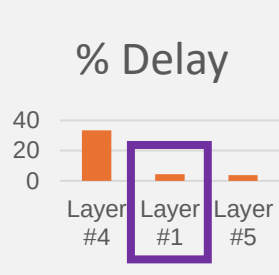
Layer CC Contribution to total RC delay

Layer name	Delay (fs)	% Delay
Layer #1	60	29.501
Layer #2	34	16.614
Layer #3	12	6.309



Layer R Contribution to total RC delay

Layer name	Delay (fs)	% Delay
Layer #4	68	33.349
Layer #1	8.9	4.382
Layer #5	7.5	3.706



Result: Located **exact polygons** in **via/metal layers** of nets for **RC delay optimization** in the delay line block, using ParagonX

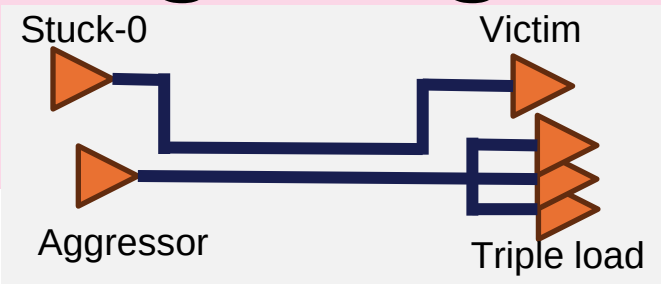
With ParagonX we found that **impact of layer #1 CC on RC Delay was greater** than that of layer #1 R

Sensitivity analysis helped locate exact polygons to be **optimized for R or CC** or both, for best RC delay optimization

4. Locate Parasitic Bottlenecks impacting Design

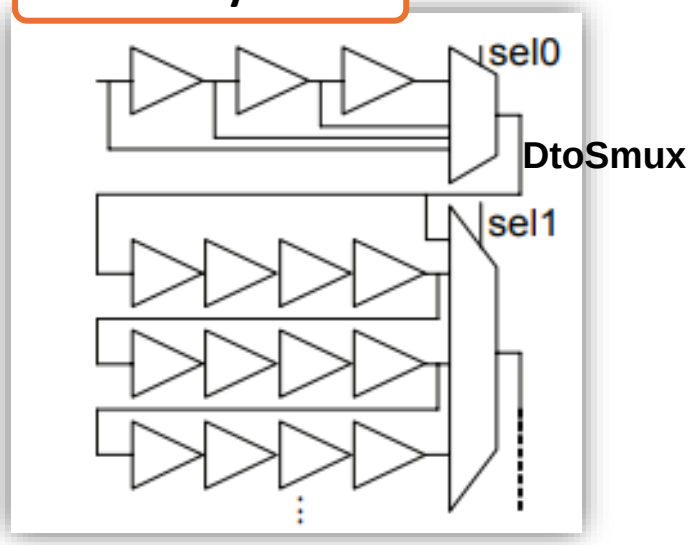
AIM: Perform **glitch analysis** of victim nets (e.g.: DtoSmux)

- Victim net waveform and pullup/pulldown glitch magnitude were reported by ParagonX



Crosstalk leads to a Glitch at the Victim cell

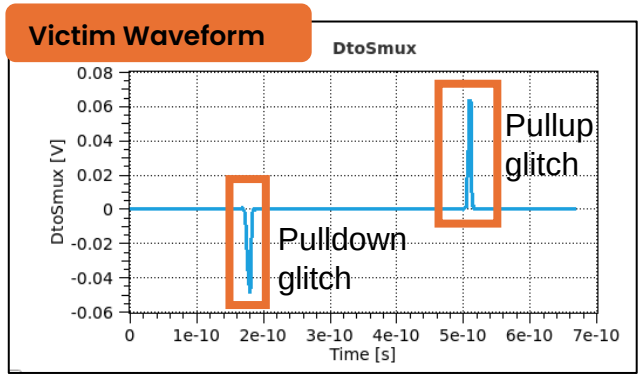
Cell: Delay MUX



Glitch Analysis Results

Node	Glitch pullup [V]	Glitch pulldown [V]
DtoSmux	0.064161	-0.049823

Victim Waveform



All Results were generated using Ansys ParagonX

Simulation setup

Victim net	DtoSmux
Simulator	Spectre
Temperature	125 C
Input ramp time	0.0146e-9 s
Period input signal	3.33e-10 s
Victim supply voltage	0.825 V
Aggressor supply Voltage	0.825 V
Glitch threshold	0.2 V
Aggressor CC/C_total threshold	0.1

Result: The glitch values and waveforms helped us quickly design/verify of our circuit.

Also, ParagonX identified the critical coupling capacitance (CC), prone to glitch. We made appropriate design modifications to reduce CC to reduce glitch.

Conclusion

- NXP is the **first** company to apply the **unique approach** of IC layout parasitics analysis to **enhance custom macro/IP/standard cell library** development flow
  - It effectively addresses our major reliability concerns, identifying probable latent defects for DFT improvements
- The very important decision of selecting the right foundry for our product was taken by **comparing 2 foundry LPE netlists**
  - Used the **powerful LPE netlist comparison** functionality of Ansys ParagonX
- **LPE netlist is no more a black-box!**
- **PDK impact analysis with ParagonX** saved us **6 months** of rework
- **Productivity improvement: 2x**
  - IC layout parasitics analysis, visualization and debugging using Ansys ParagonX
    - With ParagonX: less than 3 days; Without ParagonX: 7 days **=> 2x reduction** in std. cell design time per technology node
    - Additional savings: designer's time; simulation license cost; hardware utilization
    - enabled fast and easy identification of design bottlenecks, otherwise impossible, lowering risk of design returns

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